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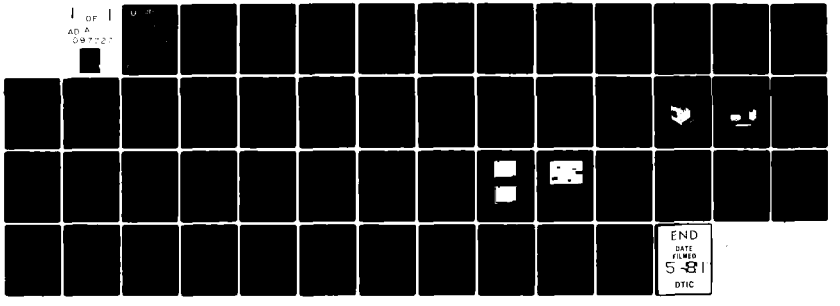

LEVEL II

12

Research and Development Technical Report
DELET-TR-79-0290-1

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HIGH CONTRAST CRT MODULE

Michael H. Kalmanash
Norden Systems, Inc.
Norwalk, Connecticut 06856

February 1981

Interim Report for Period 1 October 1979 - 31 March 1980

Approved for public release;
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Prepared For: ELECTRONICS TECHNOLOGY AND DEVICES LABORATORY

ERADCOM
US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this program is the development of a miniature high contrast color CRT module compatible with the AN/APR-39 system, except for an increase in overall length compared to the monochrome AN/APR-39 display indicator.

The initial interim period of this program has resulted in the development of an initial breadboard system, and the completion of packaging feasibility and initial design for the Advanced Development Model.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION 1
CONFERENCES

1.1 25 OCTOBER 1979 AT ERADCOM

Report of Conferences held at ERADCOM, Ft.Monmouth, New Jersey on 25 October 1979 with Norden Systems concerning contract DAAK20-79-C-0290, High Contrast CRT Module.

Personnel Present:

Norden Systems

D. Monarchie
M. Kalmanash
R. Walker

ERADCOM

E. Schlam
P. Krzyzkowski
R. Tuttle
J. Ceres

The purpose of the meeting was to review and discuss the recently awarded contract.

Basic ground rules as well as the program philosophy were discussed.

The Megatek exerciser was discussed in terms of the cost trades between the use of M-5000 modules to interface with ERADCOM's Nova computer, as proposed; and the use of a standalone unit. Norden was asked to look into this as well as whether switchable writing speeds could be provided from the Megatek, to accommodate the APR-39 V(2) mode simulation as well as the general purpose mode.

It was decided that busy signals may not be required during color switching, as defined in the Technical Guidelines, since predetermined waits can be defined in processor software.

Fabrication and sealing problems with the high contrast CRT's were discussed, and there was some question as to whether Norden or the United Technologies Research Center could provide assistance in the tube manufacture.

1.2 17 JANUARY 1980 AT ERADCOM

Report of conference held at ERADCOM, Ft.Monmouth, New Jersey on 17 January 1980 with Norden Systems concerning contract DAAK 20-79-C-0290, High Contrast CRT Module.

Personnel Present

Norden Systems

D. Monarchie
M. Kalmanash
R. Walker

ERADCOM

E. Schlam
P. Krzyzkowski

The purpose of the meeting was to discuss AN/APR-39 operating characteristics.

Strobe waveforms for the AN/APR-39(V)1 were described and it was indicated that the maximum strobe PRF was 6 kHz, not 2.5 kHz as defined in the Technical Guidelines.

In the AN/APR-39(V)2 system the maximum number of symbols to be displayed was defined as 11, with the character writing speeds about 3000 inches/second, not 50,000 inches/second as in the Technical Guidelines.

Norden was asked to review the impact of these changes on the design of the high contrast CRT module. P. Krzyzkowski indicated that the 50,000 inches/second writing speed requirement for the general purpose XY-mode may be eliminated to aid in accommodating the other changes, since this writing speed is inconsistent with 3-inch CRT display formats.

Norden was asked to investigate buying a Megatek M-701 exerciser as a standalone unit, perhaps with a Kratos color monitor as test equipment.

1.3 15 FEBRUARY 1980 AT EW LABORATORY

Report of conference held at EW Laboratory, Ft. Monmouth, New Jersey on 15 February, 1980 with Norden Systems.

Personnel Present

Norden Systems

D. Monarchie
M. Kalmanash

ERADCOM

P. Krzyzkowski

EW Laboratory

F. Szantai

The purpose of the meeting was to observe an operating AN/APR-39 system to gather data on operating parameters for the (V)1 and (V)2 configurations. The worst-case (longest) strobe times for the (V)1 mode were seen to be about 55 usec, while in the (V)2 mode the worst case symbol was a square, taking about 240 usec, with a square enclosing a character being the worst composite symbol, with a maximum of about 460 usec. The maximum number of symbols displayed per frame is eleven, with the possibility for each to be a composite symbol (i.e. an alphanumeric character enclosed in a square).

1.4 7 APRIL 1980 AT NORDEN

Report of Conference held at Norden Systems, Norwalk, Connecticut on 7 April 1980.

Personnel Present

Norden Systems

D. Monarchie
M. Kalmanash

ERADCOM

P. Krzyzkowski
E. Schlam

The purpose of the meeting was to review program status. The breadboard system was demonstrated with a Norden 5-inch by 7-inch color CRT and the color switch operating with 400 usec windows.

Problems associated with the Megatek exerciser were discussed, and Dr. Schlam indicated that he would contact Megatek and try to expedite the technical uncertainties associated with whether Megatek could meet our requirements.

It was decided that it would be permissible for the module in the (V)2 mode to operate with a regulated power interface, similar to the monochrome indicator, instead of the MIL-STD 704 interface as in the (V)1 mode.

SECTION 2
INTRODUCTION

2.1 BACKGROUND

Increased mission requirements for military aircraft warrant the use of color displays to improve identification of warning information and enhance speed and accuracy of response. Two restraints on the widespread use of cockpit color display systems have been limited display contrast available from color CRTs and concerns about the additional size, weight and power dissipation associated with the color display electronics.

Recent advances in penetration color phosphor technology have improved efficiency to the point where attainment of adequate contrast to permit operation in direct sunlight is feasible. ERADCOM has supported a more aggressive approach by sponsoring the development of high contrast beam penetration CRT screen using transparent thin film phosphors deposited over a black layer which serves to absorb incident ambient light and thus improve display contrast. The CRTs under development using the thin film high contrast screen have 3-inch diameter faceplates and use magnetic deflection, electrostatic focus guns.

In the present program, Norden System is developing an extremely compact multicolor display indicator which will utilize the high contrast CRT described above. The indicator, dubbed the High Contrast CRT Module (HCCM) is used with the AN/APR-39 radar warning system. It is housed in a form factor identical to the monochrome AN/APR-39 display indicator, but with an increase in overall length to accommodate the additional color circuitry. The HCCM is a fully self-contained unit, and meets or exceeds monochrome AN/APR-39 display operating characteristics.

The development of circuitry capable of high speed color switching and of meeting exacting standards of color registration accuracy and inter-color brightness uniformity within the power and volume restraints imposed, marks a breakthrough in display indicator technology. When completed, the HCCM development will demonstrate conclusively that cockpit color display presentations are available with minimum impact on system size, power or cost.

2.2 STATEMENT OF THE PROBLEM

The basic problem addressed by this program is the development of a high contrast display indicator capable of being demonstrated in flight in conjunction with an AN/APR-39 radar warning system. The indicator is to be compatible with both the (V)1 and (V)2 versions of this system and additionally is to operate in a general purpose X-Y mode.

Key to the success of the program is the development of a compact color switch capable of rapidly driving the CRT anode voltage through an 8 kV range. Switch size, complexity and disipation must be minimized to permit packaging within the overall module outline dimension. Additionally, switching speed and settling time must be optimized to permit writing shortly after the color switch commands.

Since the color HCCM is required to operate at anode voltages far in excess of the monochrome AN/APR-39 indicator (18 kV vs. 7.5 kV) deflection currents are intrinsically greater in the former. Care must be taken that deflection power be minimized to avoid undue thermal stresses within the box.

To attain optimum performance within the exacting guideline specified, it is an unwritten requirement that the HCCM be designed synergistically, so that operational requirements are satisfied by the functional elements in a manner that reduces parts count and power, and maximizes performance.

2.3 TECHNICAL GUIDELINES

2.3.1 Scope: High Contrast CRT Module

These technical guidelines outline a program describing the performance, design, development and testing of a CRT display module for airborne use, incorporating a newly developed high contrast CRT. The module, when interfaced to the AN/APR-39 or other similar equipment, shall provide a multi-color display comfortably legible in direct sunlight. The program objective is for the module to meet all performance guidelines enumerated herein. The module shall be designed to be electrically and physically compatible with the AN/APR-39 for test and evaluation purposes.

2.3.2 Applicable Documents

The following document of the issue in effect on the date of request for proposal form a part of this technical guidelines except as specified herein. In the event of conflict between the documents referenced herein and the content of this technical guideline, the contents of this technical guideline shall be considered a superseding requirement.

2.3.2.1 Military Specifications:

MIL-E-1	Electron Tubes, General Specification for

MIL-S-19500	Semiconductor Device, General Specification for
MIL-E-5400	Electronic Equipment, Airborne Aircraft, General Specification, for
MIL-STD-454	Standard General Requirements for Electronic Equipment
MIL-C-14806	Coating Reflection Reducing, for Instrument Cover Glasses
MIL-STD-810	Environmental Test Methods
MIL-R-49121(EL)	Radar Signal Detecting Set, AN/APR-39(V)1 (Confidential)
MIL-STD-704	Electric Power, Aircraft, Characteristics Utilization of

2.3.2.2 Other Documents

TM-11-5841-283-20	Detecting Set, Radar Signal AN/APR-39(V)1, June 1977
TM-11-5841-283-34	Detecting Set, Radar Signal AN/APR-39(V)1(U), October 1977 (Confidential)
TM-11-5841-288-34	Processor, Digital CM-480/APR-39 (V), Control, Detecting Set C-10412/APR-39(V)(U) July 1978 (Confidential)

Specification (Preliminary) - High Contrast CRT

2.3.2.3 Army Drawings

DL-SM-B-877076	Indicator, Radar Signal IP-1150/APR-39(V)
SM-D-876940	Cover, Indicator
SM-D-876950	Chassis, LH Assembly
SM-D-876953	Panel, Front
SM-D-876983	Chassis, RH Assembly

PL-SM-B-877004	Parts List, CCA Deflection Amplifier
SM-C-877014	Light, Indicator
SM-C-877040	Indicator, Radar Signal IP-1150/APR-39(V)
SM-D-877063	Printed Wiring Board HV Power Supply
PL-SM-B-877064	CCA, HV Power Supply
SM-C-877065	Transformer, HV Power Supply
SM-C-877076	Indicator, Radar Signal
PL-SM-B-877076	Parts List, Indicator Radar Signal
SM-D-877090	Power Supply Assembly, H.V.
SM-A-877100	Coil, Tube Deflection
SM-E-877284	Connection Diagram

2.4 REQUIREMENTS

2.4.1 General

This program shall be directed towards the design, fabrication and test of an advanced development model of an airborne display module that will use a newly developed high contrast multi-color CRT. The module shall consist of the 3-inch CRT, yoke, digitally controlled high voltage power supply and the necessary deflection, focus and blanking interface circuitry required to operate the module as the display indicator for present and planned versions of the AN/APR-39. It is intended as a form, fit and function retrofit for the existing module; however a slightly extra length to accommodate the switching power supply will be allowed. No external optical filters except a high efficiency antireflective (HEA) coating on the CRT faceplate are intended. Performance objectives will include, but not necessarily be limited to the features outlined in the following paragraphs.

2.4.2 Detailed Program Objectives

2.4.2.1 Performance

2.4.2.1.1 Displayed Information

The module shall be capable of displaying graphical data and alphanumeric symbology. Strobe-type displays shall be the primary graphic display consideration.

2.4.2.1.2 Cathode Ray Tube

The display device shall be a newly-developed penetration screen CRT type with superior contrast capabilities. It incorporates a transparent phosphor and black background with a nominal 3 inch diameter faceplate. Preliminary specifications for the CRT are referenced in paragraph 2.3.

2.4.2.1.3 Display Luminance

The CRT luminance as a result of signal modulation shall be sufficient to produce a comfortably legible display under dynamic writing conditions, consistent with 3.2.1.5. To this effect, each color should be capable of luminance levels of a minimum of 20 fl. The intensity of each available color is to be internally adjustable within the module to allow a single front panel mounted intensity control on the module to provide satisfactory legibility of displayed information under all ambient conditions.

2.4.2.1.4 Display Uniformity

The CRT luminance over the active viewable area, for any selected color and all colors, when operated at a set anode voltage for optimum color discrimination, shall not vary more than plus or minus 20% of the average brightness determined over the screen as determined under dynamic writing conditions.

2.4.2.1.5 Legibility

The display symbology or strobes shall be comfortably viewable at angles with plus or minus 30 degrees to the display normal under all ambient conditions from direct sunlight (10,000 fc), to moonless night conditions (.001 fc). Reflection reducing coatings such as HEA coating, per MIL-C-14806, shall be used to reduce specular reflectance at the CRT front surface.

2.4.2.1.6 Night Vision Goggles

The display should be comfortably legible with use of night vision goggles, independent of display color, and the module shall not therefore be a source of stray light under any circumstances.

2.4.2.1.7 Symbol Line Width

Symbol line width for all colors shall not exceed 0.012 plus or minus 0.004 inch when luminance is sufficient to meet the high ambient conditions at the scanning speed stated in paragraph 3.2.1.8.

2.4.2.1.8 Writing Conditions

The luminance and line width requirements shall be measured under typical AN/APR-39 display conditions. A 20,000 in/sec scanning speed at 2.5 kHz refresh, 12% duty cycle, for all colors for strobe displays and a scanning speed of 50,000 in/sec at a 50 Hz refresh rate, 1% duty cycle for all colors for symbology could be typical.

2.4.2.1.9 Spot Position

The center of the nondeflected, focused spot for all color fields shall fall within a circle of 1/16 inch radius concentric with the center of the tube face, with the tube shielded. X and Y deflection centering controls shall be screw driver adjustable to the optical center of the display, internal to the module if required.

2.4.3 High Voltage Power Supply

2.4.3.1 Physical Size

The anode power supply shall be designed to fit within the overall dimensions of this module. Some allowance is permitted for lengthening of the overall module, maximum increase not to exceed 3 inches. This power supply shall be encapsulated for electriclal isolation and environmental conditions. It is desireable that the anode supply be contained within a single housing.

2.4.3.2 Anode Voltage Levels

Two anode ranges shall be provided. A voltage range of approximately 10 kV to 18 kV is of primary concern and a reduced voltage range of approximately 7 kV to 12 kV is of secondary concern. The two ranges may be incorporated into a single supply or interchangeable single range units may be utilized. Each voltage range shall be capable of four voltage levels, each level coincident with a different defined color from the CRT. Intermediate voltage levels shall be internally adjustable.

2.4.3.3 Anode Current Characteristics

The anode current supply should be sufficient to operate the CRT consistent with the preliminary CRT specifications (2.3) and paragraph 3.2.1.

2.4.3.4 Color Control

Means shall be provided and contained within the module to digitally control the anode voltage level with a two bit TTL command. This control signal shall be interfaced to th rear of the module in the form of a standard connector or incorporated into the main module interface connector. A test point is desirable to monitor the anode voltage without direct connection to the high voltage output.

2.4.3.5 Anode Voltage Switching Time and Repetition Rate

The switched anode voltage level shall reach 0.5% of its final value in 75 usec. Switching or repetition rate of the supply shall be considered in relation to the AN/APR-39 system. A maximum repetition rate is desirable in addition to the above characteristics.

2.4.3.6 Anode Voltage Switch Busy Signal

Means shall be provided in the form of a TTL level signal, to sense when the anode voltage power supply is in the switching mode in order to disable data flow until a quiescent voltage level as per 3.2.2.5, is reached.

2.4.3.7 Input Power

The anode power supply shall operate from typical +28 Vdc aircraft power supplies as per MIL-STD-704. Total current drain should be less than 1 amp.

2.4.3.8 Output Voltage Characteristics

Regulation to line or load shall be 0.5% or less. Output ripple at all voltage levels shall be 0.1% peak to peak or less.

2.4.3.9 High Voltage Output Connector

A standard high voltage output connector, such as AMP 832692, shall be used to connect to the anode lead of the CRT.

2.4.4 CRT Sensitivity Correction

2.4.4.1 Deflection Sensitivity Correction

Means shall be provided within the module to electrically correct for the change in deflection sensitivity with anode voltage change. Such correction should be controlled from the color bit input signals and result in a maximum convergence error not to exceed 0.006 inch anywhere over the usable area of the screen.

2.4.4.2 Focus Sensitivity Correction

If necessary to meet the requirements of 3.2.1.7, means shall be provided within the module to electrically correct for the focus sensitivity change with anode voltage. It is desirable that focus sensitivity correction be controlled from the color bit input signals.

2.4.5 Controls

The module front panel shall include only a single luminance control. The luminance of the display shall be continuously variable to meet paragraphs 3.2.1.5 and 3.2.1.6 in less than one revolution of the control knob.

2.4.6 Module Signal Input Interface

The module shall be capable of functioning as the display module for the AN/APR-39 system at given anode voltage, and interface through the approved connector 2JI, as per Drawing SM-C-877040.

2.4.6.1 APR-39 Deflection Interface

The deflection interface of the subject module shall be compatible with the current deflection interace of the AN/APR-39 as noted in Para. 3.5.1.6.1 of MIL-R-49121(EL), 10 Mar 1977 Confidential.

2.4.6.2 General Purpose Deflection Interface

In addition to the special APR-39 deflection system, a general purpose deflection system, shall also be provided. To this effect, a random scan mode of operation using X & Y bipolar voltage deflection signals compatible with conventional random scan display generators (see deliverable item #3) shall be incorporated. It is desireable that such incorporation be included in the module, with the two deflection schemes conveniently switchable, however this added capability may be included in a minimal sized add-on, or as two separate modules. These alternatives should be analyzed in the proposal.

2.4.6.3 Unblank Interface

The unblank interface of the module shall be compatible with unblank characteristics of the AN/APR-39 as noted in TM-11-5841-283-20.

2.4.6.4 Missile Alert Light

The missile alert light shall meet the requirements set forth in paragraphs 3.2.1.5 and 3.2.1.6.

2.4.7 Service Conditions

It shall be considered a goal of this program that the module be designed for quality and environmental standards comparable to that of the existing AN/APR-39 indicator module.

2.4.7.1 Environmental

Although qualification testing is not part of this program, the module should be designed and fabricated to meet certain environmental conditions as noted in MIL-STD-810, specifically:

Vibration: Method 514.2, Procedure I, Part I, Curve B (2g)

Shock: Method 516.2, Procedure I, in accordance with Figure 516.2-2 for flight vehicle equipment.

Temperature-Altitude: Method 504.1, Procedure I for Class 5 equipment is in accordance with Table 504.1 for equipment in the non-operating simulated 40,000 feet above sea level mode shall be used.

Humidity: Method 507.1, Procedure II, with test measurement Step 4 and during the last five hour period of the fifth 48-hour in step 6. Moisture accumulation on the face of the module shall not constitue failure of test.

2.4.7.2 Primary Power

The module shall remain safe and operate normally under changes in prime power as per MIL-STD-704 and MIL-R-49121(EL). It is desirable that the module power supply current be minimized when operated at the nominal +28 Vdc normal aircraft operating voltage.

2.4.7.3 Form Factor and Weight

The module shall be identical to the existing AN/APR-39 module as per TM-11-5841-283-20, with some allowance for greater length (see 3.2.2.1) and weight, if necessary.

2.4.7.4 Electrical Connections

The electrical connections on the module shall be compatible with AN/APR-39 system as per paragraphs 3.2.5.

2.5 TESTING, DOCUMENTATION AND DRAWINGS

2.5.1 General

It shall be a requirement of this program that sufficient engineering drawings and complete documentation covering all components, assemblies and circuitry be included to enable follow-on programs by qualified system contractors.

2.5.2 Performance Testing

An appropriate number of modules shall undergo engineering testing to assure that they meet the requirements of these guidelines, and all data shall be appropriately recorded. Tests shall include transfer characteristics and tolerance limits on all interfacing parameters to insure that tolerance limits are adequate to insure module interchangeability. Paragraphs 2.4.1.2, 2.4.2.1.3, 2.4.2.1.4, 2.4.2.1.5, 2.4.2.1.6, 2.4.2.1.7, 2.4.3.5, 2.4.3.7, 2.4.3.8, 2.4.4.1, and 2.4.7.1, shall be emphasized.

2.5.3 Module Display Scenarios

Static displays of typical AN/APR-39 scenarios shall be provided and utilized for evaluation and demonstration of the capabilities of the display module when operated in the AN/APR-39 modes.

SECTION 3
TECHNICAL APPROACH

3.1 FUNCTIONAL DESCRIPTION

The HCCM is an extremely compact four color stroke write display indicator. The functional architecture of the unit is illustrated in Figure 1.

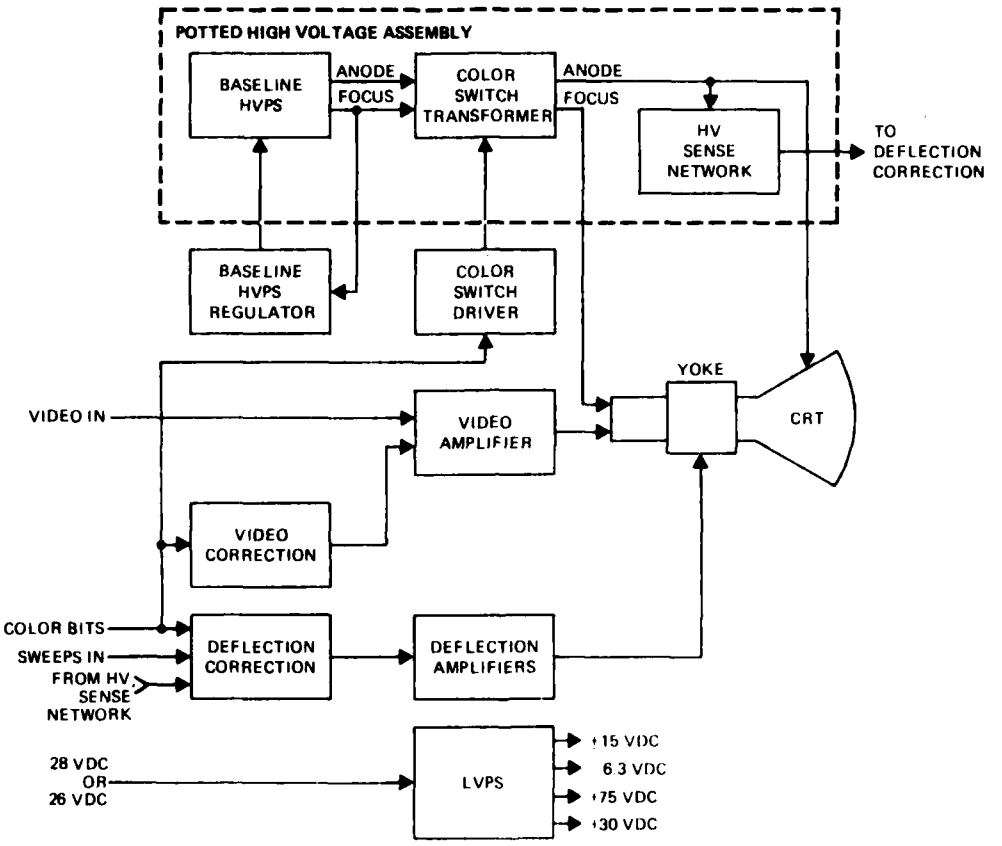


Figure 1. HCCM Functional Block Diagram

Anode voltage for the CRT is derived from a color switch transformer whose output is offset by a baseline HVPS. The color switch output dynamic range is plus or minus 4 KV around the baseline HV output, while the latter is itself adjustable from 10 KV to 18 KV. For monochrome operation, such as in the APR-39(V)1 mode, the color switch transformer output is held at zero, and the baseline HVPS output is varied between 10 KV and 18 KV to produce the different colors. For multicolor operation such as in the APR-39(V)2 mode, the baseline HVPS output is set to 14KV

and the different colors are addressed dynamically by the color switch transformer. The anode voltage range 10-18 KV is accessed by dynamically operating the switch transformer in the range plus or minus 4 KV. This transformer is under control of the color switch driver which sets up the required waveforms in response to incoming color bits.

The anode voltage is sensed and used to provide dynamic control of the deflection sensitivity as a function of color. Regulation of the baseline HVPS is provided by sensing the baseline focus output voltage.

Deflection system sensitivity is maintained by a combination of programmed gain adjustment as a function of color bits, and linear correction based on dynamic sensing of the actual CRT anode voltage. The deflection amplifiers are current sinking amplifiers driving a 4-winding push-pull deflection yoke. Power dissipation is minimized by maintaining zero quiescent current in the deflection amplifiers. Deflection system power dissipation is thus a function of display load.

An internal LVPS operates from the line voltage and generates all the regulated voltage required for the HCCM.

3.2 INTERFACE DESCRIPTION

The HCCM interface is shown in Figure 2 and is in two parts; the operator interface and the electronics interface. The operator interface consists of the brightness control and the MODE control. The brightness control varies the gain of the video amplifier. Internal circuitry adjusts the gain as a function of color such that brightness uniformity between colors is maintained over the entire range of the brightness control.

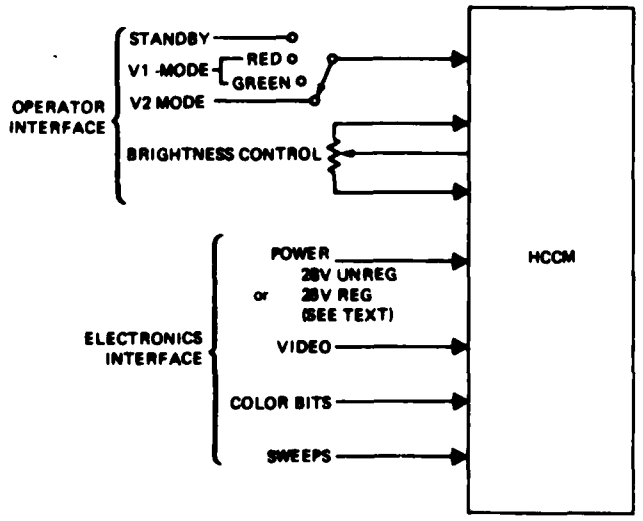


Figure 2. HCCM Interface

The MODE control selects between V1 and V2 modes of operation, and serves basically to set the color levels on the HCCM. Since the V1 mode is monochrome, selection of this mode disables the color control circuitry from the incoming color bits. Instead, color (RED or GREEN) is determined by the position of the MODE control when selecting V1 mode. In the V2 mode, color is determined by the incoming color bit pattern, which selects between RED, ORANGE, YELLOW, and GREEN. Additionally, a standby mode position is provided, in which the CRT anode voltage is held at zero.

The electronics interface to the HCCM consists of power and signal lines. The power interface is from a single DC source. In the V1 mode, this source is unregulated 28 Vdc (per MIL-STD-704), while in the V2 mode the HCCM interfaces with a 26 Vdc regulated source. This difference is primarily due to the need to limit power dissipation in the V2 mode by limiting input voltage excursions, much the same as in the monochrome V2 system.

The video input signal is a TTL compatible unblanking signal which gates the video amplifier. CRT drive is internally adjusted as a function of color to maintain intercolor brightness uniformity.

The deflection inputs are differentially received in the HCCM. As illustrated in Figure 3, the four sweep inputs from the AN/APR-39 system are combined into two bidirectional signals, horizontal and vertical. Color correction is applied to these signals and they are then channelled into four unidirectional signals to drive the yoke. In the random scan XY-mode, the horizontal and vertical sweep signals are applied directly to the horizontal and vertical receivers. The coordinate transformation shown between the random scan and AN/APR-39 display modes may be effected by a 45 degree rotation of the yoke.

Three color bits interface the HCCM. The two color control bits determine the color to be displayed, however the actual high voltage transition does not occur until the enable bit is activated. This initiates the write/reset timing cycle described in Section 4.1.3.

DIFFERENTIAL RECEIVER	DISPLAY CONFIGURATION	
	AN/APR-38	RANDOM SCAN
HORIZONTAL	FR AL	X X-RETURN
VERTICAL	FL AR	Y Y-RETURN

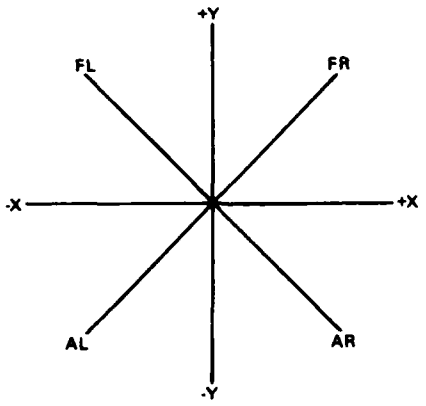


Figure 3. Input Sweeps

SECTION 4
TECHNICAL STATUS

4.1 BREADBOARD

The electrical design of the HCCM is complete. A preliminary breadboard system has been integrated using a Norden 5-inch by 7-inch CRT, and is illustrated in Figure 4. The breadboard demonstrates the required performance from the video and deflection systems, and the internal low voltage power supply. Electrical performance of the preliminary color switch has also been verified but verification of a reduced size, extended performance configuration for the high voltage magnetics is underway.

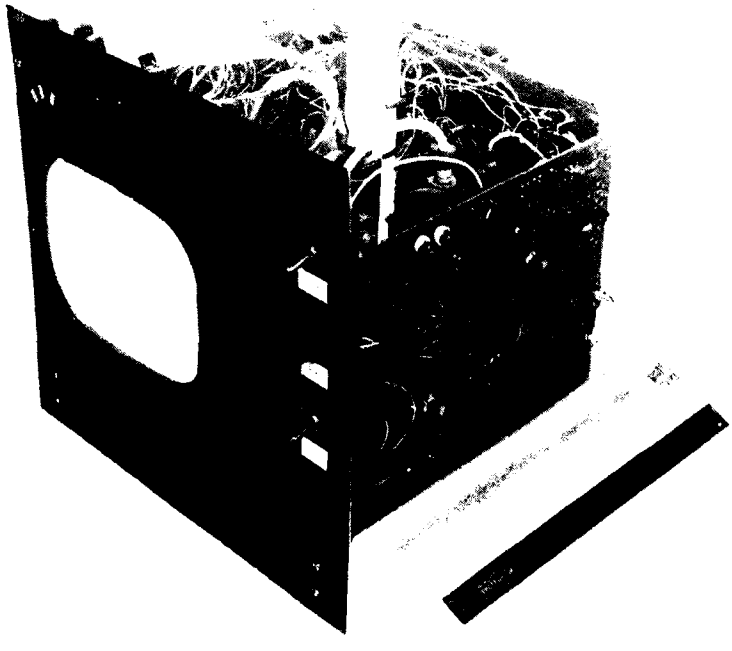


Figure 4. Preliminary HCCM Breadboard

The original performance characteristics specified in the Technical Guidelines have been extended for both the V1 and V2 modes of operation. In the V1 mode, the change has been an extension of deflection system power dissipation due to an increase in maximum sweep PRF from 2500 HZ to 6000 HZ. In the V2 mode the changes have been a re-interpretation of symbol writing time, to a maximum of nearly 400 usec per symbol (a worst case

being an alphanumeric character enclosed in a box), whereas initially the worst case display load was taken as 200 usec per frame (1% duty cycle at 50Hz refresh). The impact of this change is an increase in deflection amplifier power due to higher duty cycle, and an increase in color switch power due to wider windows and higher duty cycle. While it appears that the higher dissipation can be accommodated within the box, this comes at the expense of larger heat sink area which leaves a correspondingly smaller volume to be allocated to the high voltage assembly. To accommodate this, the size of the baseline HVPS transformer has been reduced, and the intent is to accommodate the wider color windows in the color switch transformer without an increase in size of this element. Verification of performance under these conditions by further breadboard fabrication and test is underway. The original breadboard high voltage magnetics assemblies are illustrated in Figure 5.

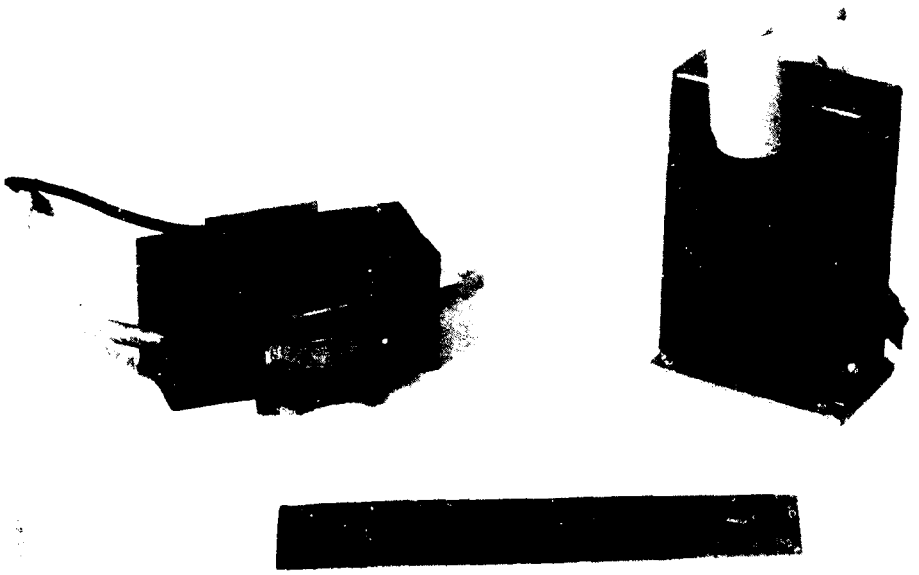


Figure 5. Original Breadboard HV Magnetics Assemblies

4.1.1 Video Amplifier

The breadboard video amplifier receives digital unblanking and color bit information and generates grid and cathode output waveforms to drive the CRT. Special circuitry ensures brightness uniformity for all four colors at all

brightness levels. Additional circuitry has been added to the video amplifier for the purpose of protecting the CRT phosphor from damage due to abnormal loss of power or loss of deflection sweeps.

Unblanking drive is provided to the CRT from a wideband cascode output stage (see Figure 6). The output stage gain is controlled by the front panel brightness pot, R11, whose effect is modulated by the incoming color bits via U2 and R5, R6 and R7. This modulation is necessary to adjust CRT beam current as a function of color, and thus maintain inter-color brightness uniformity.

Sweep fail protection is provided in that the screen is blanked when writing speed sensors on the deflection amplifiers indicate loss of sweeps or when thermal switches indicate a potential thermal overload. Under this condition, the color switch drivers are disabled through circuitry on the video amplifier board.

4.1.2 Deflection System

For simplicity and direct compatibility with the 28vdc line, the HCCM uses a four-winding push-pull deflection yoke driven by four identical single-ended current-sinking feedback amplifiers (A6, A7, A8, and A9) as in Figure 7. The voltages across the yoke windings are sensed individually and combined to give a composite indication of loss of sweeps to blank the video amplifier, if necessary.

The input sweeps are differentially received in a manner compatible both with random scan XY deflection inputs and with AN/APR-39 sweep inputs. In the random scan X-Y deflection system there are two bipolar inputs, one for each sweep axis; while in the AN/APR-39 configuration there are four sweep inputs, each representing one of the intercardinal radials. By rotating the deflection yoke 45 degrees for the AN/APR-39 configuration, the following equivalence can be established.

Random Scan	AN/APR-39
+X	FR
-X	AL
+Y	FL
-Y	AR

Thus, the following inputs may be provided to the horizontal and vertical receivers, provided the yoke is rotated for the AN/APR-39 configuration.

	Display Configuration	
Receiver	Random Scan	AN/APR-39
Horizontal	X	FR
	X-RETURN	AL
Vertical	Y	FL
	Y-RETURN	AR

The outputs of the receivers (A1 and A2)in either configuration are then bipolar signals which are acted on by the color sensitivity correction circuitry comprised of A3, A4, and A5. Electronic centering is provided by R2 and R47 to maintain the position of the undeflected spot in the center of the screen within 1/16 inch. The centering inputs are provided to the differential receivers (A1 and A2) before the color correction circuitry (A4 and A5).

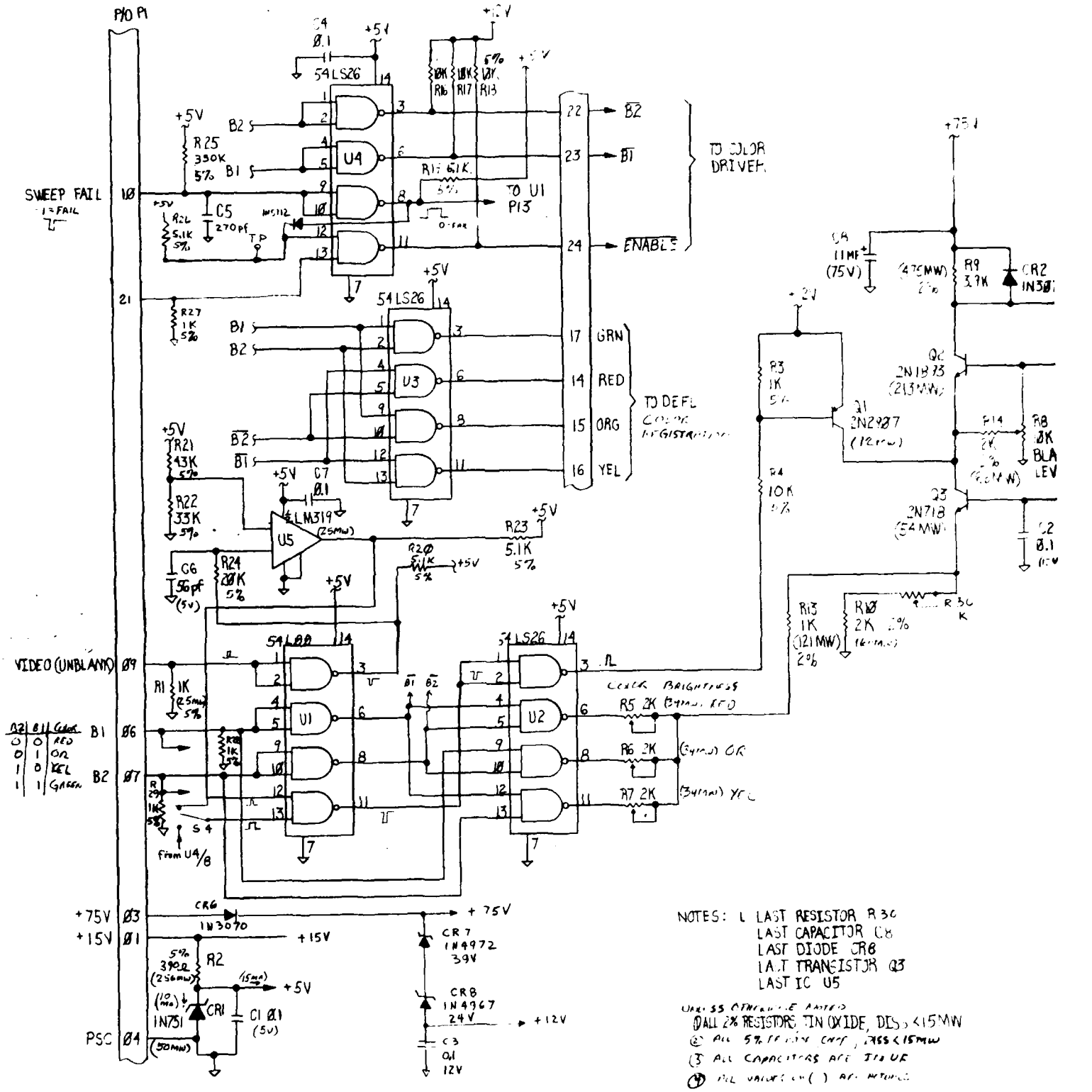
It is known that magnetic deflection channel sensitivity varies as an inverse function of the square root of the anode potential and therefore that color displays require correction of this sensitivity change to ensure proper display color registration. The conventional approach toward this problem is to adjust the deflection amplifier gain by a fixed amount as a function of the selected color, but Norden has in the course of past color experience developed a patented approach for correcting color sensitivity which has many advantages over the conventional approach. The Norden approach, as used in the HCCM, consists of sensing the instantaneous anode potential in a wideband compensated, buffered voltage divider and applying this signal to a wideband, accurate square root network and then to multipliers that generate the corrected signals. The general equations for the corrected signals are:

$$Xcorr = X \ \text{sqrt}\ (HVn)$$

$$Ycorr = Y \ \text{sqrt}\ (HVn)$$

where sqrt (HVn) is the square root of the normalized anode potential. In the HCCM deflection system, this function is performed by A3, A4 and A5 which serve to perform the square root function and modulate the horizontal and vertical gains, respectively.

The bipolar color corrected signals out of A1 and A2 are converted to push-pull waveforms by phase splitter circuitry(A5 through A9) and are then applied to the yoke driver amplifiers. The driver amplifiers are Q1, Q2, A6; Q3, Q4, A7(horizontal),


P10 P1
SWEEP FAIL
1=FAIL
10
21
VIDEO (UNBLANK)
09
B1
06
B2
07
PSC
04
+75V
03
+15V
01
54LS26
54LS00
U1
U2
U3
U4
U5
TO U1 P13
TO COLOR DRIVER
TO DEFL
GRN
RED
ORG
YEL
ENABLE
CLOCK BRIGHTNESS
From U4/8
CR1
IN751
CR2
IN3070
CR7
IN4972
39V
CR8
IN4967
24V
Q1
2N2907
Q2
2N1893
Q3
2N718
LM319
NOTES: 1 LAST RESISTOR R30
LAST CAPACITOR C8
LAST DIODE CR8
LAST TRANSISTOR Q3
LAST IC U5
UNLESS OTHERWISE NOTED
2 ALL 2% RESISTORS, TIN OXIDE, DISS < 1/5 MW
3 ALL CAPACITORS ARE 35 V DC
4 ALL VALUES IN ( ) ARE NOMINAL

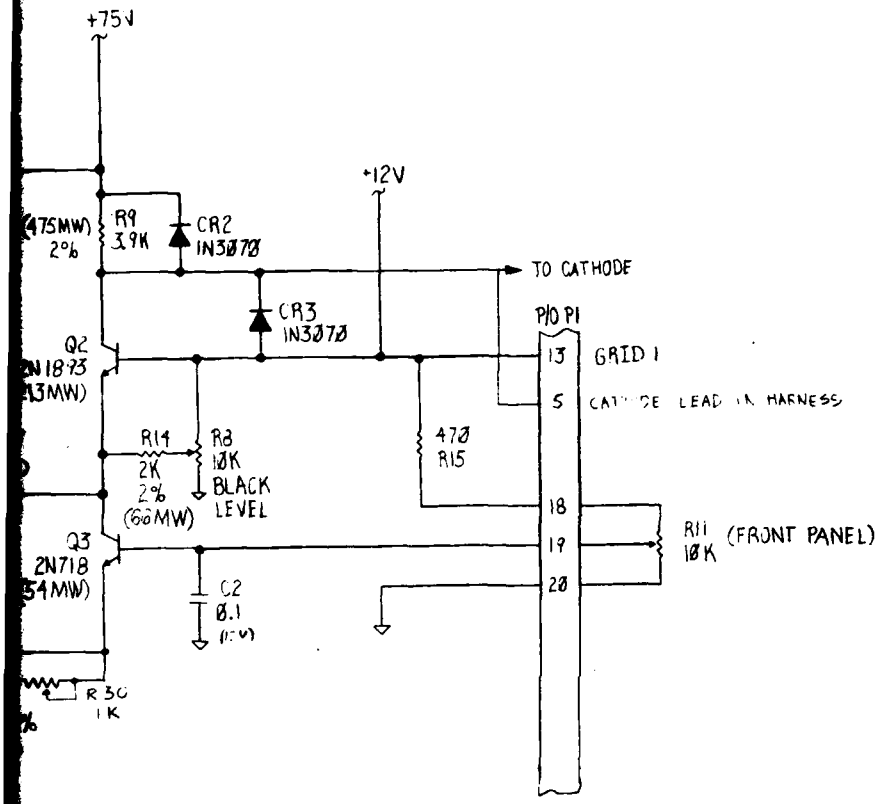
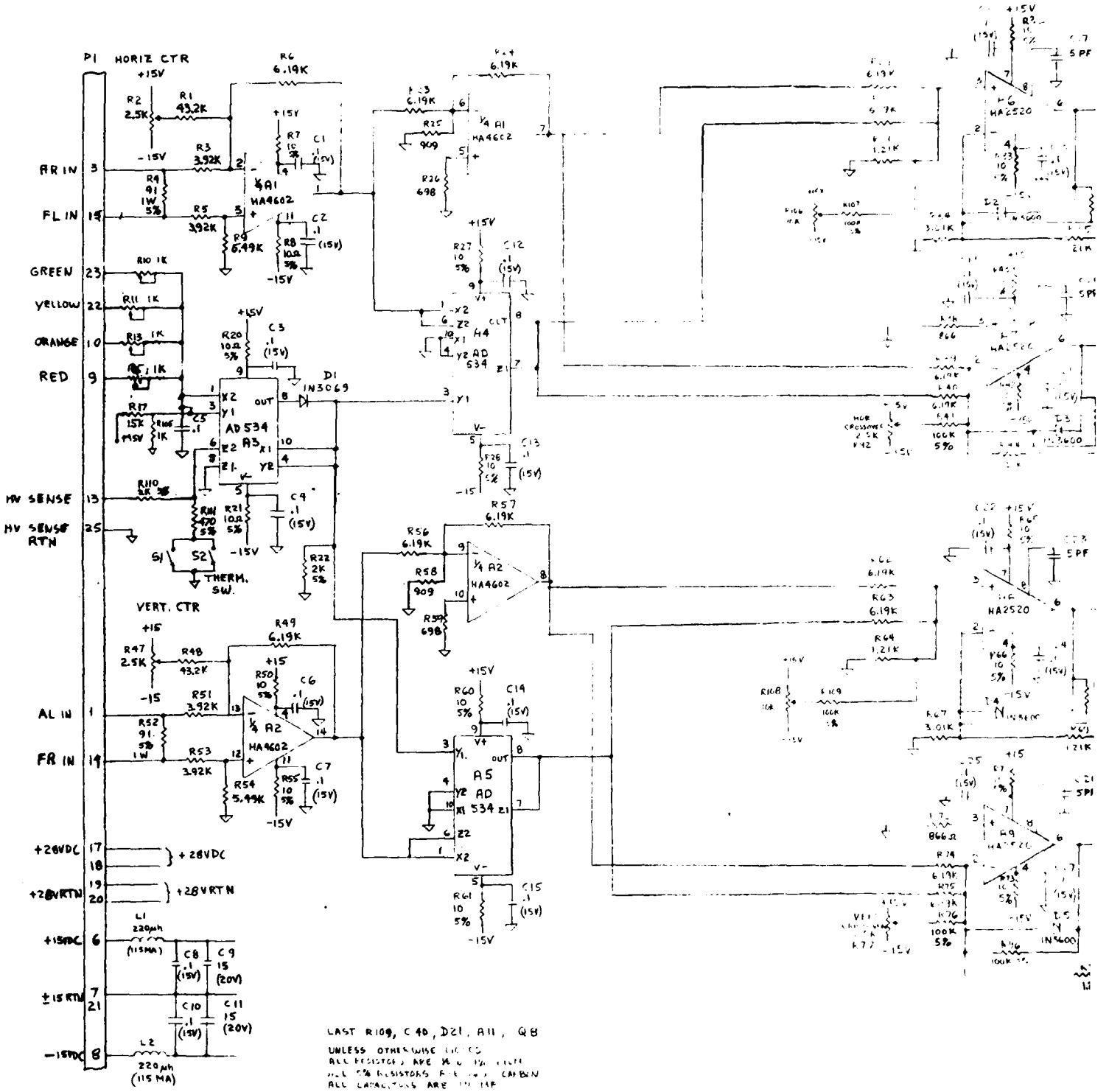


Figure 6. HCCM Breadboard Video Amplifier


P1 HORIZ CTR
VERT. CTR
HR IN
FL IN
GREEN
YELLOW
ORANGE
RED
HV SENSE
HV SENSE RTN
AL IN
FR IN
+28VDC
+28VRTN
±15VDC
±15 RTN
-15VDC
THERM. SW.
AD 534
HA4602
HA2520
LAST R109, C40, D21, A11, Q8

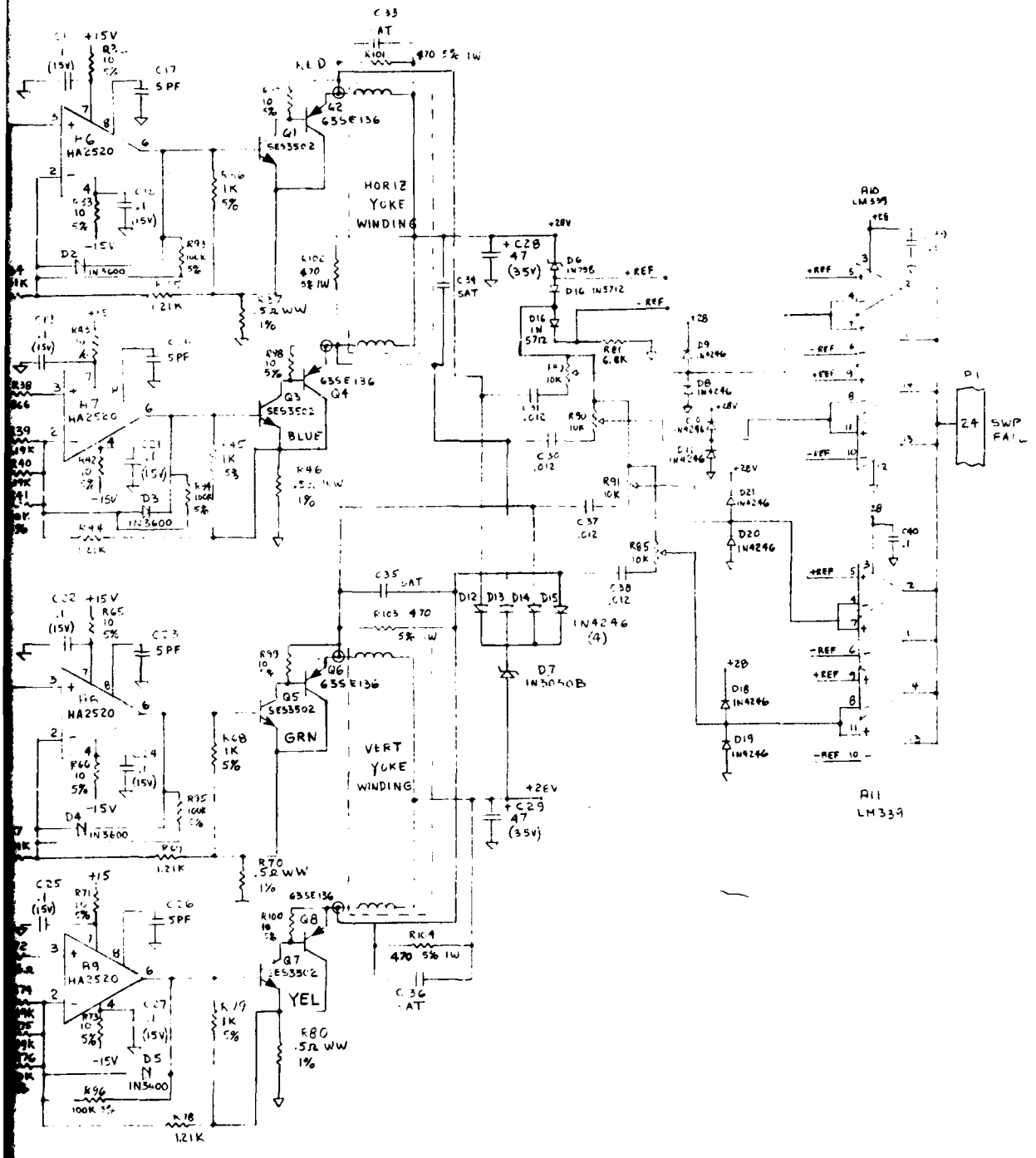


Figure 7. HCCM Breadboard Deflection System

7

andQ5, Q6, A8; Q7, Q8, A9 (vertical). Only one driver amplifier of each pair (horizontal or vertical) is providing yoke current at a given time, depending on beam position on the screen. Therefore the phase splitter circuitry maintains zero quiescent current in the unused driver amplifier, thus minimizing power dissipation.

Power dissipation in the HCCM deflection amplifiers is a function of display load, due to the driver quiescent current being zero. In the V1 mode, therefore, the extension of worst case strobe PRF from 2500 Hz to 6000Hz implies an increase in deflection system power of 240%. A similar increase occurs in the V2 mode where the 1% duty cycle called in the Technical Guidelines is extended by more than an order of magnitude because of the slower character writing speed and larger character writing times. To accommodate this increase within the physical constraints of the HCCM, the yoke inductance was raised to lower the deflection currents. The revised system is fully capable of simulation of the APR-39 V1 and V2 modes. While some reduction in power dissipation results from the yoke re-definition the net power is still greater than originally, and additional heat sink area is still required. Quantitatively, the deflection system power figures are given in Figure 8.

The HCCM deflection yoke, while similar to that used in the monochrome AN/APR-39 indicator, is made smaller to permit more room for the additional color circuitry required for the HCCM. Within this constraint, the determination of optimum yoke inductance was made based on consideration of writing speed and power dissipation.

	Original System	Increased Requirements	Redesigned System
PRF	2500 Hz	6000 Hz	6000 Hz
Yoke Inductance	100 uH	100 uH	100 uH
Deflection Power	16.0 W	38.5 W	23.9 W

Figure 8. Deflection System Power, V1 Mode

The deflection yoke for the HCCM has been developed by Display Components, Littleton Ma. The original breadboard HCCM deflection yoke had an inductance of 100 uH per winding, which was sufficiently low to support a writing speed of 50,000 inches/second per the technical guidelines, according to the relation:

$$E = LdI/dt + IR$$

where E is the minimum voltage available to the yoke, L is the yoke inductance (100 uH), I is the yoke current, and R is the yoke resistance. When the yoke was redefined as described above, the design criterion was to maximize inductance (minimizing system power) commensurate with the Vl writing requirements of 20,000 inches/second at 18KV.

Key parameters of the original monochrome AN/APR-39 yoke and the two HCCM yokes are given in Figure 9.

	Monochrome AN/APR-39 Yoke	Original HCCM Yoke	Final HCCM Yoke
Mechanical			
OD(max).	2.391"max.	1.875"max.	1.875"max.
ID(min).	.930 min.	0.984"min.	0.984"min.
Length	1.5"	1.5"	1.5"
Deflection Angle	70	70	70
Electrical			
Push-Pull Windings	Yes	Yes	Yes
Inductance	480 uH	100 uH	265 uH
Winding Resistance	3.3 ohms	0.75 ohms	1.76 ohms
Peak Current (at 18KV)	1.28A	3.7A	2.22A

Figure 9. Yoke Comparison

4.1.3 Color Switch

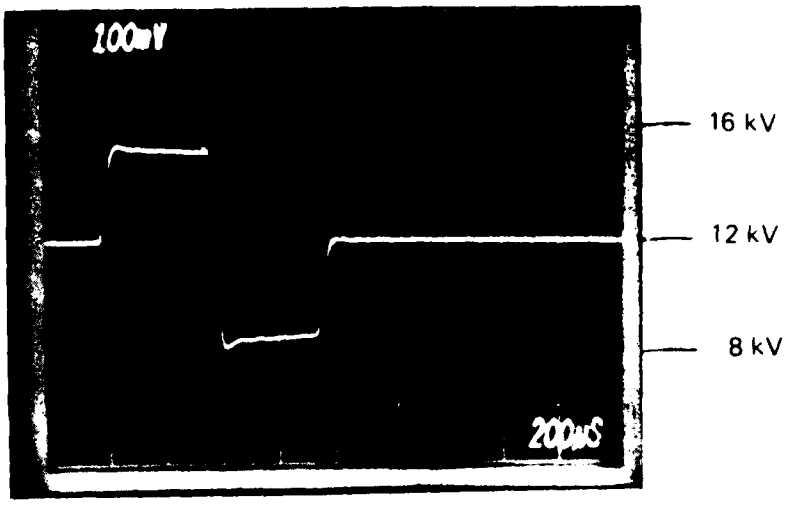
The color switch consists of a regulated baseline HVPS providing a pedestal level for a dynamic color switch transformer.

Operation of the color switch is based on the COLOR WINDOW principle, where a given color is accessed for a given time period (WRITE window), sufficient to write a block of data. This is followed by another interval (RESET window) typically blanked, where the color switch transformer is reset. The timing of the WRITE and RESET windows is controlled within the HCCM.

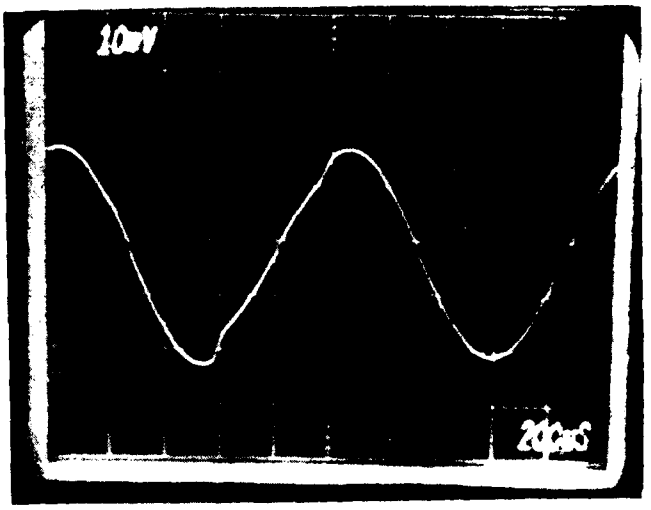
Typical operation of the color switch is shown in Figure 10. The upper waveform is the actual anode waveform. The WRITE window width is 400 usec and the color switching time for a 4 kV transition is less than the required 75 usec. The baseline level shown in the figure is 12 kV. In the ADM units this will be 14 kV.

For reference, the lower waveform of Figure 10 shows the yoke output voltage in response to a sinusoidal input (writing a circle on the screen), during a color transition. Note the discontinuities in the waveform which illustrate the effects of the color sensitivity correction circuitry acting on the deflection amplfiers.

Figure 11 illustrates an actual circle drawn on the CRT screen. The circle is written with color switching as in Figure 10 applied to the display. In actual operation, the display would be blanked for about 75 usec following the start of the WRITE window and during the RESET and BASELINE intervals, but here the display is intentionally left unblanked to illustrate the quality of the color switching and correction. Note the absence of visible ringing and large color switching transients on the screen. Even the RED-GREEN (WRITE-RESET) transition which is only partially corrected since it is typically blanked, is free from significant aberrations. For reference, the entire circle is written in one millisecond.



a. Anode HV Waveform



b. Color - Corrected yoke Waveform (Sine Wave)

Figure 10. Color Switch Waveform

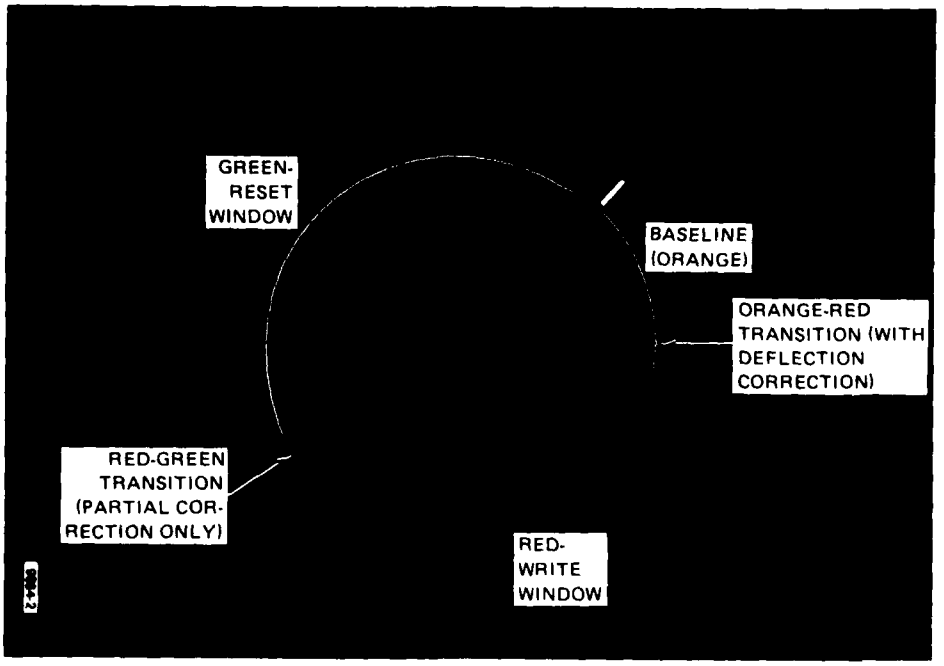


Figure 11. Dynamic Color Switching Display

The current breadboard color switch is capable of operation with 400 usec color windows, at plus or minus 4 kV amplitude. This represents an interim step in meeting the revised technical guidelines.

The original Technical Guidelines specified a 1% duty cycle for multicolor symbology. With a 50 Hz refresh rate, this represents 200 usec writing per frame. The original breadboard version of the HCCM color switch was therefore configured to be capable of 200 usec WRITE windows, with up to four or five color switching cycles per frame. An interim discussion revealed that the character times were perhaps 200 usec each, which led to wider WRITE windows to permit blanking of the color transitions, and also raised the number of color switching cycles per frame to equal the number of charactes (up to ten). This represents the current breadbord status. A later conference (15 February 1980, at EW Laboratory, Fort Monmouth) revealed that the maximum symbol time could be about 460 usec, prompting a further redesign of the color switch to accommodate 600 usec windows(to allow for color transition time, plus a margin). A breadboard version of this final configuration is presently being implemented.

The impact of these changes has been two-fold. Since the color switch circuitry is only active during the switching cycles, the power dissipation has been dramatically increased as the duty cycle has grown from 1% to nearly 25%. Besides the duty cycle impact, the wider windows have led to an increase in transformer magnetizing current levels which also lead to an increase in power dissipation. Overall worst case HCCM power dissipation is now estimated at 54.6 watts, taking into account increases in color switch and deflection power dissipation. Box dissipation originally proposed was only 33.9 watts. This increase has required a thermal redesign of the box, with larger area being devoted to heatsinks, and correspondingly less volume available to the high voltage magnetics. Effort was also required to redefine the color switch circuitry to accommodate the higher power levels. Based on extensive analytical and experimental redesign efforts, the feasibility of meeting the revised guidelines seems assured.

The color switch transformer contains a primary winding and two secondary windings, one each for anode and focus drives. A critical item in the transformer design has been the choice of core material. The prime criterion for selection of the optimal core material is the saturation flux density, since flux density levels in the core follow the relationship:

$$V = NAdB/dt$$

where,

V = applied voltage

N = number of turns

B = flux density excursion

t = time (window width)

A = core cross-section area

The larger the saturation flux density, the larger can be made B, and the correspondingly smaller the core cross section area, A, can be made for an overall reduction in color switch transformer volume.

Several candidate materials were investigated for the color switch transformer core. Ferrites were rejected early because of limited saturation flux density, leaving several tape wound cores under consideration: Deltamax, Silectron, Supermendur and Metglas (alloy 2605 SC). The first three are available from Arnold Engineering Co., Marengo Illinois, among others while the latter is available from Allied Chemical Co., Morristown, N.J. Relative properties of the different candidate core materials are summarized in Figure 12.

Note the significantly lower core loss figure for the Metglas material. Core loss is expressed here as watts/cubic centimeter, rather than the more common watts/pound, since volume and not weight is the critical parameter in the HCCM.

While it remains a promising material, the Metglas alloy has not been used for the color switch transformer. The primary reason for this is that it is available only as a toroid or other uncut core, which makes packaging efficiency for a high voltage transformer so poor as to negate its other advantages which include high permeability as well as low core loss. In the future, when cut cores are available, then this material will once again become a viable candidate.

Of the remaining materilas, Supermendur was selected for the HCCM since it had the highest saturation flux density and therefore represented the smallest possible transformer. From a cost standpoint this material is significantly more expensive than the others, and Silectron might bear investigation in a production configuration where materials costs would be more significant.

	Material			
	Silectron	Deltamax	Supermendur	Metglas
Saturation				
Flux Density (K Gauss)	19.7	16.	23.	16.
Core Loss				
Watts/CC (@ 10 KGauss,60 Hz)	1.91	1.46	2.44	0.57

Figure 12. Candidate Color Switch Core Materials

4.1.4 Power Supplies

The original concept proposed for the HCCM power supplies used a single regulator operating on a fixed 14 kV high voltage output with tracking focus, G2 and LVPS outputs.

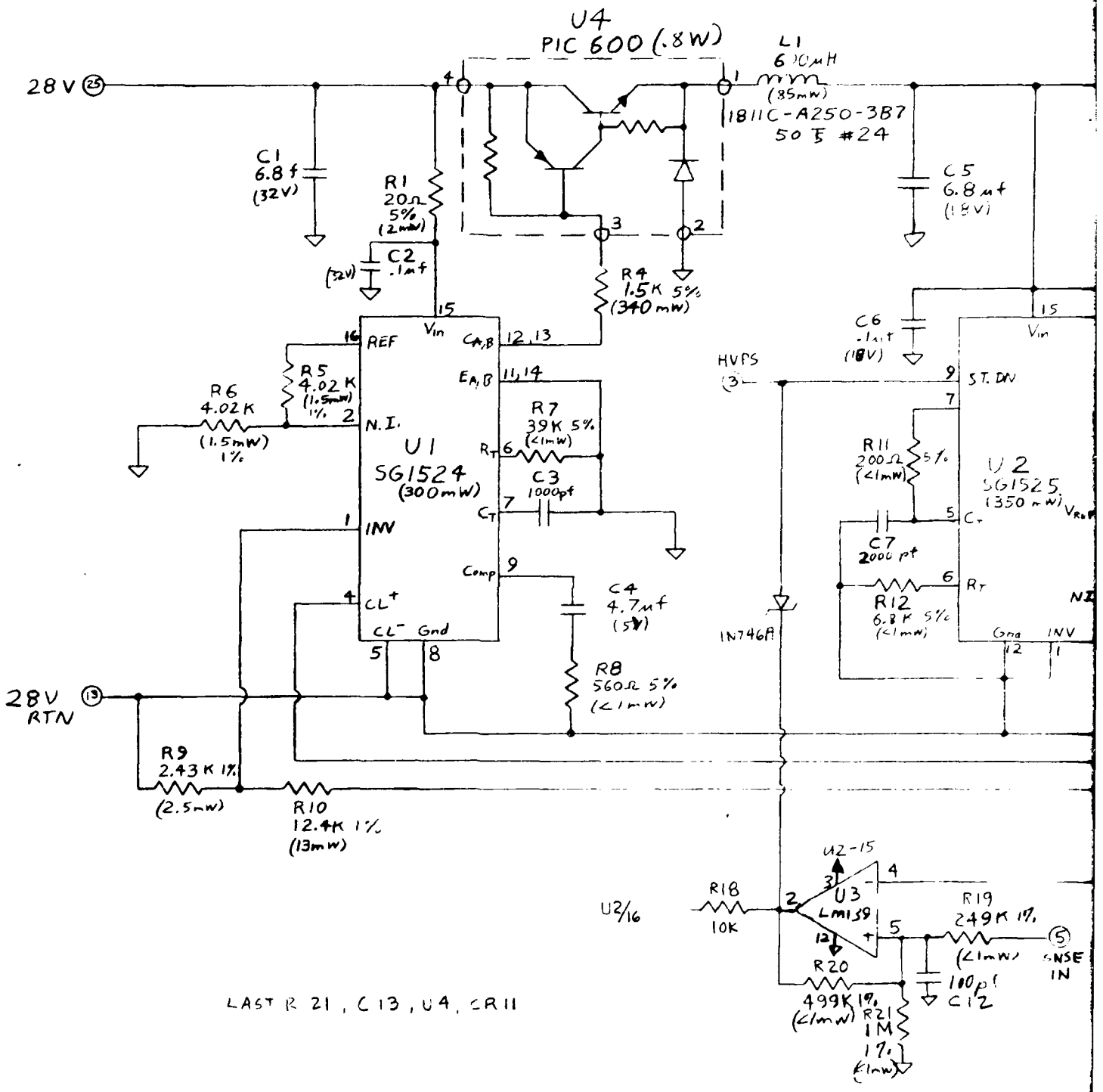
Early in the program it was recognized that for flexible V1 mode operation, the baseline HVPS had to be capable of being varied in the range from 10 kV to 18 kV. This requirement invalidated the concept of other outputs tracking the anode output and mandated separation of the high voltage and low voltage power supplies. The operation of the low voltage power supply may be understood with the aid of the schematic of Figure 13. Referring to this figure, the elements U1, U4, L1 and C5, comprise a switching buck regulator which feeds the center tap of transformer T1. T1 is driven at a 40 kHz rate (25 usec period) with a 2 usec dead time for safe operation of Q2 and Q3. The integratd circuit U2 generates the base drive signals for Q2 and Q3. Feedback is provided from the +15 Vdc output to the inverting input pin 1 of U1. The reference signal is internally generated within U1, and is scaled and routed to the non-inverting input pin 2.

Overload protection is provided by using the measured primary current of T1 through the source leads of Q2 and Q3, across R16, to shut down U1. Overvoltage protection is provided by comparison of the -6.3 Vdc output (through R17) to the high voltage feedback sense (through R19); an overvoltage condition of either signal will cause pin 2 of U3 to open and shut down U2 via input pin 9. An overvoltage condition of either the high voltage or low voltage outputs will therefore shut down both supplies.

Operation of the baseline HVPS may be understood with the aid of Figure 14. Here a switching buck regulator is used to drive a single-ended flyback converter which generates the high voltage anode and focus outputs.

The flyback drive transistor Q1 is normally driven at a fixed frequency, fixed duty cyle, by the two-comparator network (output pins 1 and 2 of U2) and regulation is achieved by feedback of the focus voltage to U1 which controls the DC input to T1. The third comparator (U2 output pin 14) provides a soft start at turn-on and normally remains off thereafter. In the event of failure of the buck regulator, however, if full input voltage is passed through to T1, this comparator will operate to pulsewidth modulate the base drive of Q1, and high voltage regulation will continue (with somewhat degraded performance).

High voltage overload sensing is achieved by measurement of primary loading current across R14. Excessive current will cause shutdown via pin 4 of U1. Overvoltage shutdown is achieved via pin 10 of U1, the actual error sensing being made within the low voltage supply electronics.



LAST R 21 , C 13 , U 4 , CR 11

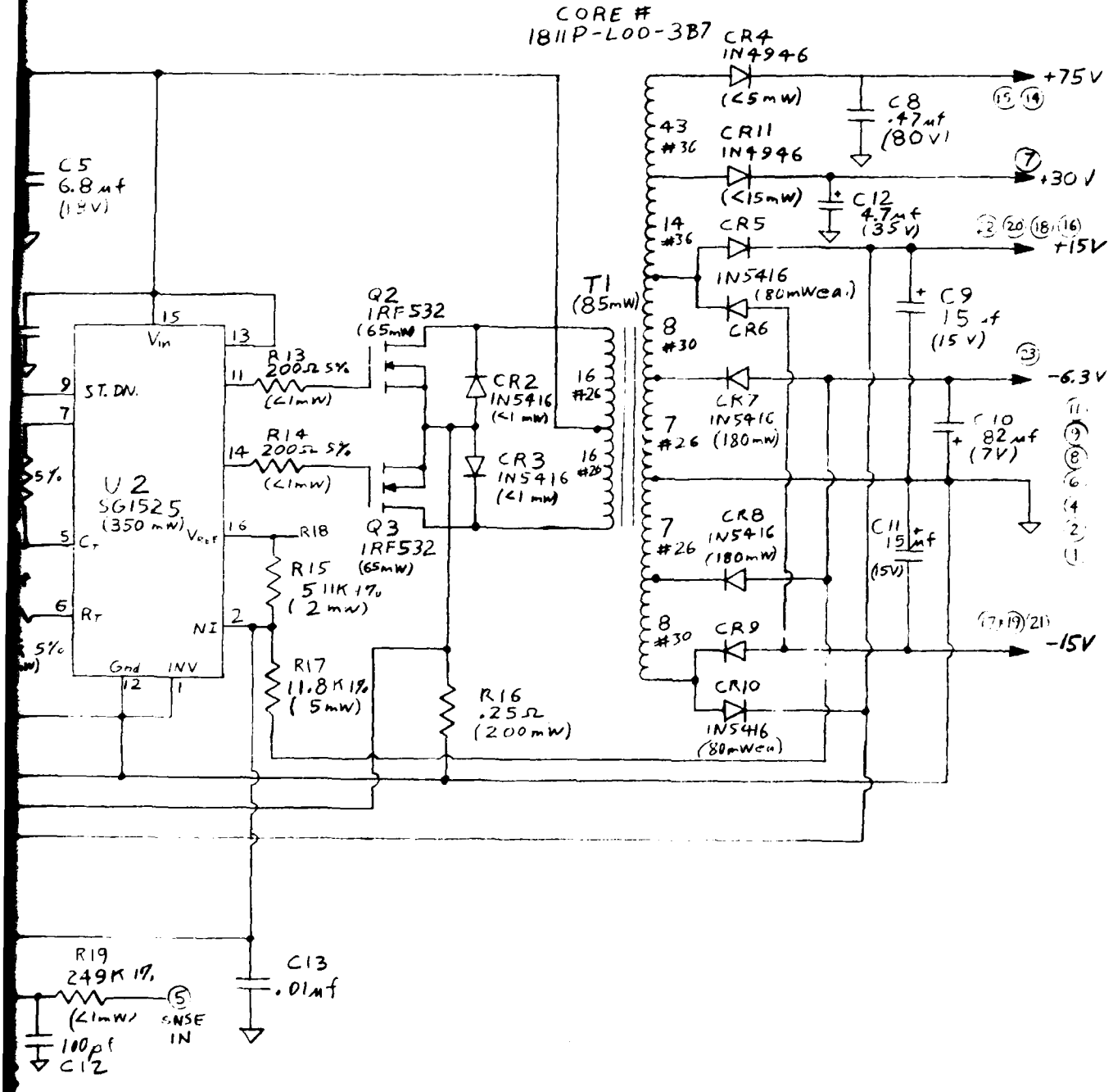
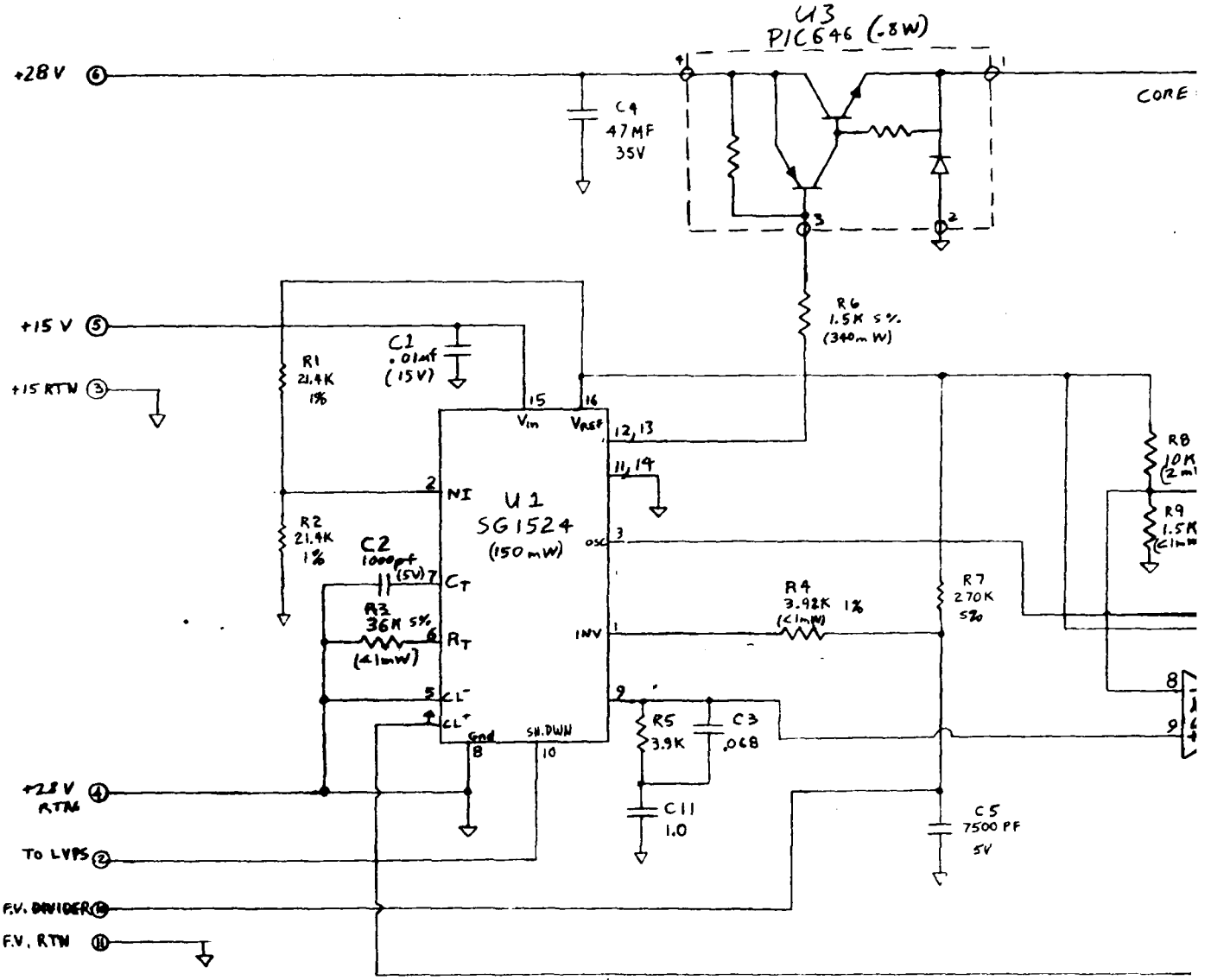
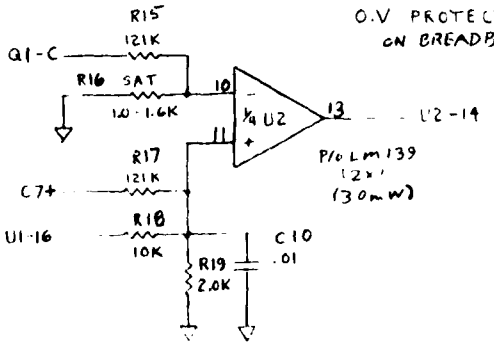


Figure 13. HCCM LVPS

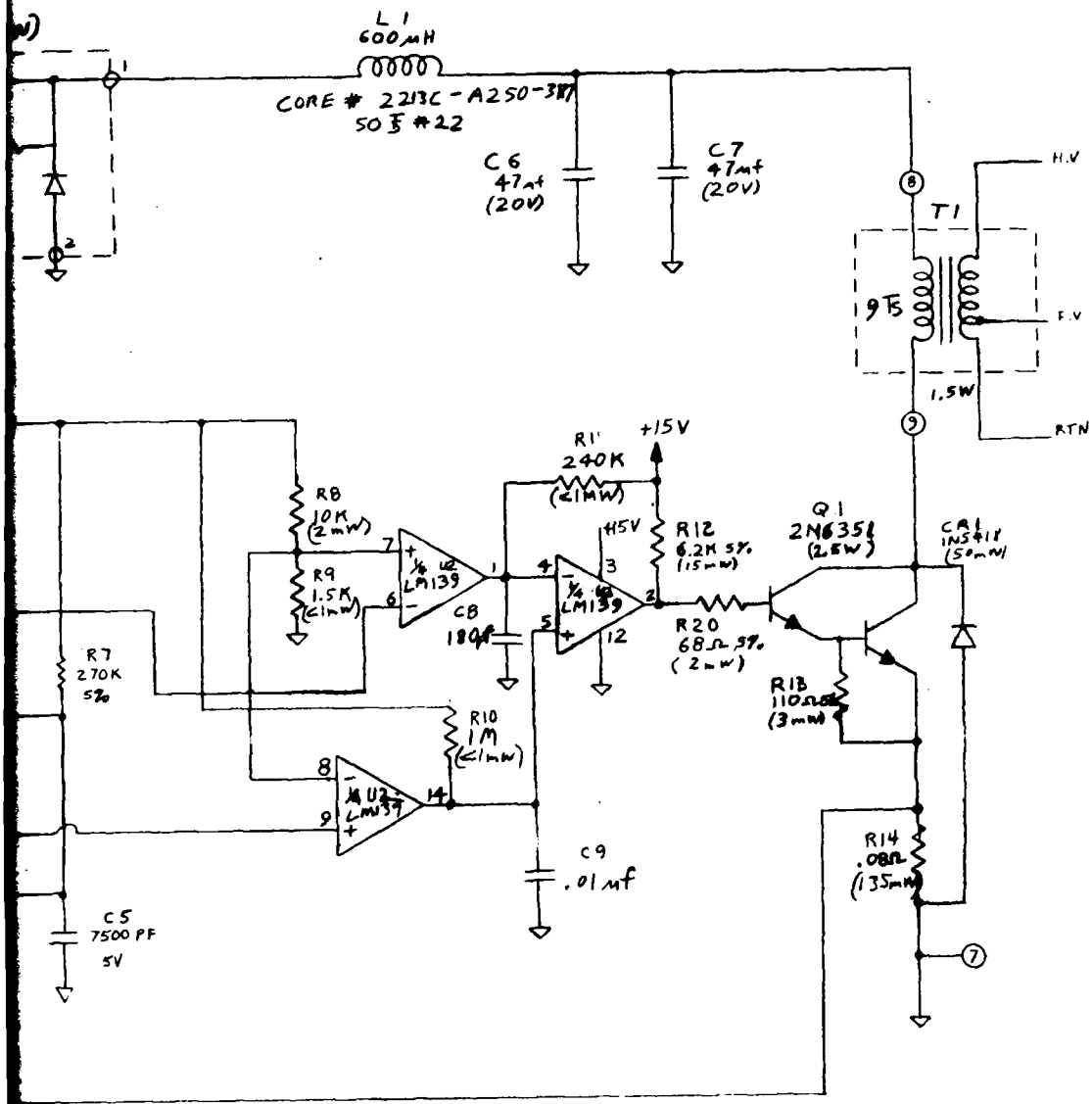


LAST R 20, C 10, U3, Q1, L1, CR1



O.V PROTECTION
ON BREADBOARD

Figur



O.V. PROTECTION
ON BREADBOARD

13 ——— U2-14

P/O LM139
(2x)
(30mW)

Figure 14. Baseline High Voltage Power Supply

The high voltage transformer itself is an adaptation of the multilayer transformer rectifier assembly described in the technical proposal. The secondary winding is comprised of 12 layers, each layer coupled to the other by a single diode as shown in Figure 15.

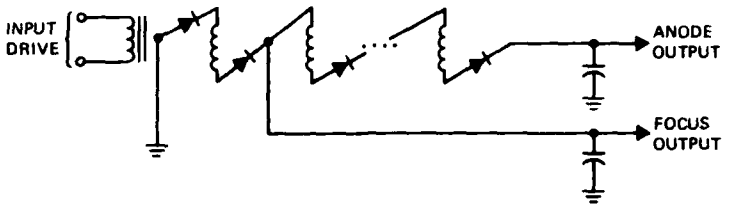


Figure 15. Multilayer Transformer Rectifier Assembly.

The use of multiple diodes, rather than a single high voltage diode, decouples the transformer layers when Q1 is on, thereby reducing reflected leakages reactance and minimizing parasitic oscillations usually associaied with high turns ratio transformers.

The breadboard supply was fabricated using bobbins and a custom core available from spare in-house supplies. This approach was taken in order to be able to use existing encapsulation molds rather than proceed directly to a new mechanical layout and fabrication cycle prior to breadboard test and evaluation. Consequently the breadboard transformer is almost four times greater in total volume than the anticipated final design. The smaller size of th final design should also further reduce leakage reactance. In all other essential aspects, the final trnasformer will be a simple dimensional miniaturization of the breadboard assembly.

4.2 ADVANCED DEVELOPMENT MODELS

The conceptual design for the Advanced Development Models (ADM's) is complete. Five printed wiring assemblies are anticipated, in addition to a high voltage assembly and the CRT assembly. A drawing of the proposed ADM construction, showing module partitioning and placement is given in Figure 16.

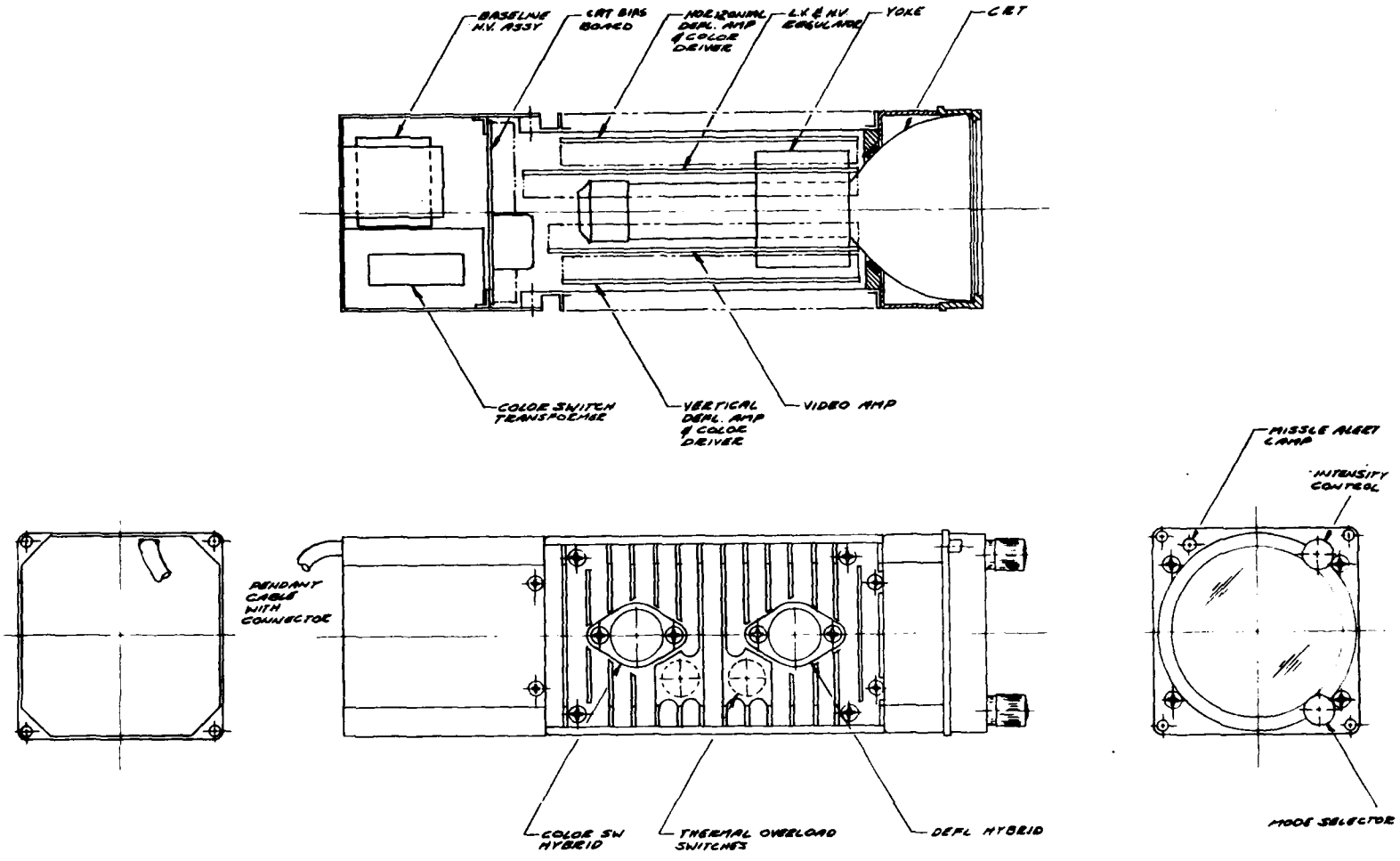


Figure 16. Advanced Development Model

Note that each of the Deflection/Color Driver boards contains an integral heat sink which houses two TO-3 devices. Each of these is a dual darlington transistor hybrid package, one each for each deflection channel and for each color driver half. Thermal switches mounted to each heatsink sense abnormal thermal stresses and respond by putting the HCCM into a low dissipation state, removing drives from the color switch circuitry and reducing deflection circuit gain to limit peak yoke currents. Upon removal of the thermal stress, the box automatically returns to normal operation.

In addition to the conceptual design, actual printed circuit board design has begun. The detailed design of the high voltage assembly will await the completion of breadboard testing of the reduced size high voltage magnetics elements.

In operating with the AN/APR-39 (V)1 system, the HCCM will interface directly with a MIL-STD-704 28VDC power source, however because of the increased power dissipation discussed above for the (V)2 mode the module will require a regulated power source for (V)2 mode of operation. Use of a regulated power source for this mode minimizes unnecessary dissipation which would be required by the need to accommodate the steady-state excursions of MIL-STD-704.

SECTION 5
CONCLUSIONS

The first interim period has demonstrated the feasibility of the basic concepts to be used in the HCCM.

Working breadboards of the required HCCM circuitry have been developed and demonstrated and the basic architecture appears to lend itself to extensions of the performance requirements as described herein.

The concepts being reduced to practice in this program should form the basis for a new class of miniature multicolor display indicators. The color switch has been demonstrated in operation performing in excess of original design goals with wider color windows; and representative test waveforms have been demonstrated in the breadboard system, verifying operation of the deflection, video, and power supply assemblies.

Packaging of the Advanced Development Models is proceeding and there is every indication that these units will function sucessfully within outline dimensions compatible with the Technical Guidelines, and meet all performance goals.

SECTION 6
PROGRAM FOR NEXT INTERIM PERIOD

The next interim period should see completion of the design of the Advanced Development Models (ADMs) and verification of performance of the electronics assemblies. Integration and delivery of the first ADM unit should follow shortly the end of the next interim period.

It is intended to repackage the breadboard unit modules in a new housing prior to delivery to ERADCOM. The new housing will offer improved personnel safety and a package more suitable for demonstration and evaluation.

Overall, six ADM units will be fabricated and made available for ground or flight evaluation, compatible with both the AN/APR-39 (V)1 and (V)2 configurations.

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